

# ***Mounting Considerations for Medium Power Surface Mount RF Devices***

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## ***Abstract:***

Traditionally, devices in the RF transmit chain dissipating more than 2 Watts of DC power have been packaged in hermetically sealed, flange mount packages. This technique provides a high level of thermal reliability, but requires extra board space and expensive manual assembly. Additionally, special care must be taken during the design of the heatsink to ensure leads from the flange mount package are critically placed on the top surface of the printed circuit (pc) board. Today, device manufacturers provide many medium power (1-4 Watts RF and 2-8 Watts DC) devices in surface mount QFN (quad flat, no lead) plastic encapsulated packages. QFN packages are provided in 3 x 3 mm to 8 x 8 mm form factors with a ground paddle. The ground paddle is exposed on the backside of the package and is inset from the outside of the part by 1 mm per side. These packages allow for surface mount assembly, an excellent thermal path to ground, and costs that can be an order of magnitude lower than hermetically sealed flange mount packages. The trade-off is that the pc board must be properly designed to dissipate heat generated by the device. This paper describes a pc board design achieving a thermal impedance of 2-4 °C/W through a 1.6 mm (0.063 in) thick FR-4 pc board—a reliable, low cost solution.

## ***Background:***

Device reliability is directly influenced by junction temperatures within device structures. Device manufacturers perform accelerated life testing on die at elevated temperatures to establish operating conditions that ensure reliable performance. Several empirical techniques are available to measure device junction temperatures including IR (infra-red) scanning, liquid crystal imaging, and measuring the change in device forward-bias voltage drop as a function of temperature. Analytical methods including finite difference and finite element techniques are also employed to predict device temperatures. Generally, empirical techniques are performed on die that are eutectically attached to infinite heatsinks so that the thermal impedance of the die alone is measured. After the thermal impedance of the die is known, the manufacturer determines the additional resistance of the package and the attach material (generally conductive epoxy or a eutectic alloy like AuSn). This is then added to the thermal impedance of the die to determine the overall thermal impedance of the packaged part.

Manufacturers often report two values for thermal impedance ( $\theta$  or “theta”):  $\theta_{ja}$  (junction to ambient) and  $\theta_{jc}$  (junction to case).  $\theta_{ja}$  is reported for devices mounted to convectively cooled pc boards while  $\theta_{jc}$  is reported for devices mounted to conductively cooled pc boards. The Electronic Industry Alliance (EIA formerly JEDEC Solid State Technology Association) has established a standard testing methodology (reference JESD51) for

determining  $\theta_{ja}$  for packages on air cooled pc boards so devices from different vendors may be compared consistently.

Most manufacturers determine  $\theta_{jc}$  either analytically or empirically by mounting the device on an infinite heatsink and measuring the

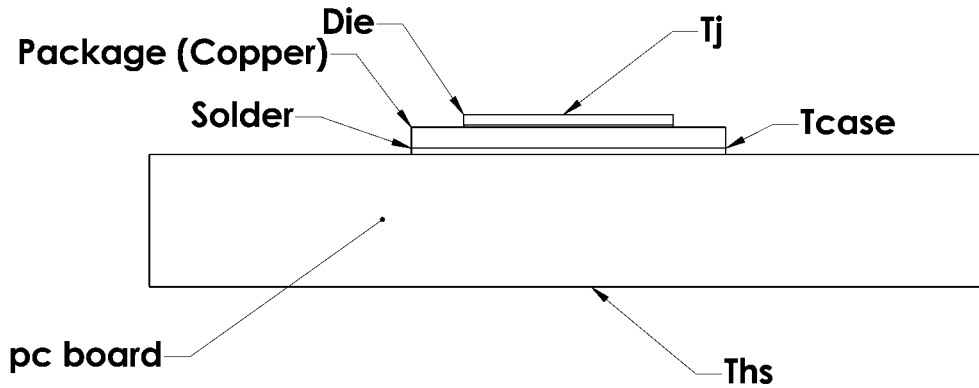


Figure 1: Cross Section of a Typical Component Mounted onto a pc Board

temperature differential between the hottest junction and some external point on the package lead frame. This article focuses on  $\theta_{jc}$  since medium power devices require conductive cooling.

The customer is left with the task of determining the actual junction temperature of the device in the field. The customer should provide a metal heatsink directly underneath the pc board which is maintained at a specific temperature (Figure 1). For this case, the junction temperature ( $T_j$ ) is determined from:

$$1) \quad T_j = T_{hs} + Q * (\theta_{jc} + \theta_{sld} + \theta_{pcb})$$

Where:

$T_{hs}$  = Heatsink temperature

$Q$  = Net power dissipated = dc power – (RF output – RF input)

$\theta_{jc}$  = Thermal impedance, junction to case

$\theta_{sld}$  = Thermal impedance of the solder

$\theta_{pcb}$  = Thermal impedance of the pc board

The device vendor provides  $\theta_{jc}$  as described above,  $\theta_{sld}$  is determined from the equation below:

$$2) \quad \theta_{sld} = \Delta x / (kA)$$

Where:

$\Delta x$  = Thickness of solder joint ( $\approx 75$  microns)

$k$  = Thermal conductivity of the solder ( $\approx 50$  W/m $^\circ$ K)

A = Area of solder coverage under the package

Methods for determining the thermal impedance of the pc board are presented in the following sections.

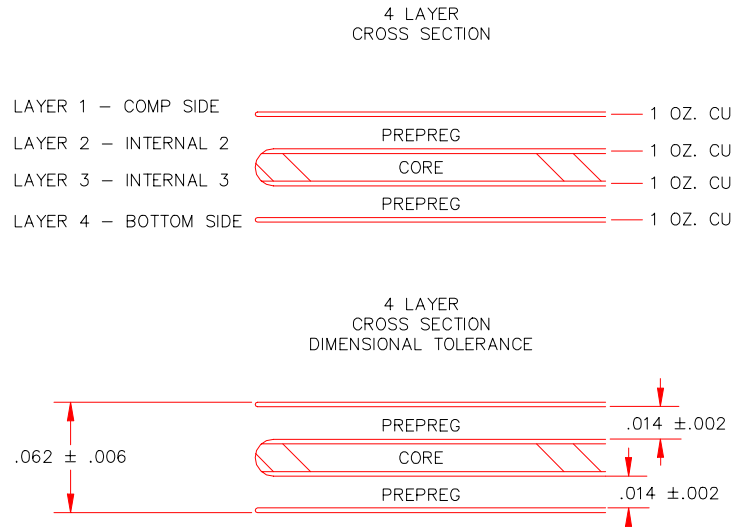
***Recommended PC Board Layout:***

The WJ AH201 is an example of a 6 x 6mm QFN package with an exposed backside die paddle. It nominally dissipates 4 W of dc power. The backside of the part is shown in Figure 2. Historically, this type of medium-power, surface mount part would have been provided in a flange mount package.



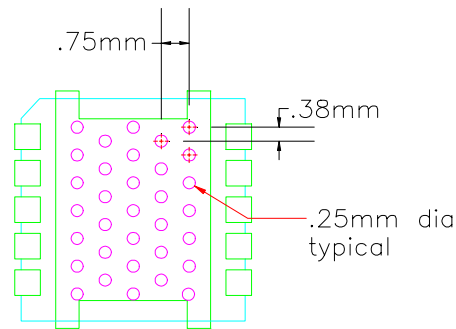
**Figure 2: Backside View of 6mm x 6mm QFN Package with Exposed Ground Paddle.**

The AH201 and similar QFN parts are designed to be soldered to FR4 pc boards with at least two separate copper layers each using a minimum of 1 oz copper. Additional copper layers can be provided, where possible, to further improve the thermal spreading characteristics of the pc board. The cross section of a typical board is shown below in Figure 3.



**Figure 3: Cross Section of pc board**

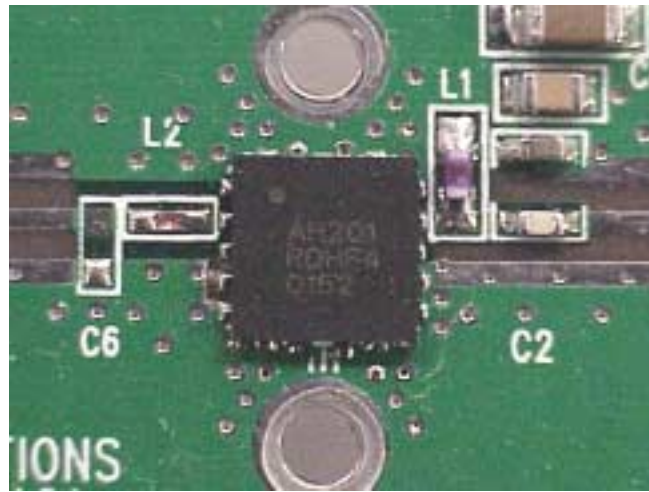
An array of 0.25 mm (10 mils) diameter finished size via holes should be provided directly underneath the ground paddle to connect the top-side ground plane to the back side of the board (heatsink). These thermal vias conduct heat from the paddle into the layers below the top side of the board. The vias should be spaced in offset rows with a spacing of 0.75 mm (30 mils) between columns and 0.38 mm (15 mils) between rows. The recommended board mounting configuration is shown below in Figure 4.



**Figure 4: Recommended pc board Mounting Configuration**

Vias placed directly underneath a component can cause solder to flow away from the ground solder joint. Surface mount assembly houses have many practical solutions for this issue. One typical solution is to enlarge the solder stencil where possible around the part and to place polyimide tape on the backside of the part. During re-flow the enlarged solder pattern allows solder to flow into the joint as it fills the vias while the tape prevents solder from flowing over the back of the board. Soldermask over the backside of the board should not be used as it will act as an insulator between the backside copper ground plane and the heatsink. In lieu of unfilled thermal vias, some customers choose to either fill the vias with conductive materials prior to assembly or to press metal inserts

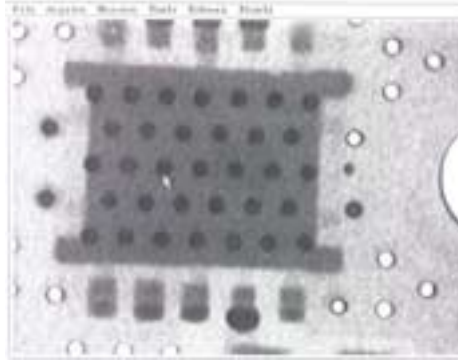
into the pc board. Figure 5 and Figure 6 show a typical QFN package (WJ AH201) assembled onto a pc board, and Figure 7 shows a cross sectional X-Ray image of a typical solder joint.



**Figure 5: PC board Assembly.**



**Figure 6: Backside of pc board Assembly (Note the Thermal Vias).**



**Figure 7: X-Ray Image of a Typical Solder Joint**

### ***Thermal Data:***

The thermal impedance of the pc board can be determined analytically or empirically. If the copper die paddle of the package is assumed to be isothermal with uniform power deposition, then a closed-form calculation can be made to estimate the thermal impedance of the board on a per via basis. From basic heat transfer, the temperature increase across a uniformly heated section with parallel heat transfer paths is:

$$3) \quad Q = k_{eq} * A_{eq} * (\Delta T / \Delta x)$$

Which may be rewritten as:

$$4) \quad \Delta T / Q = \Delta x / (k_{eq} * A_{eq}) = \text{Thermal Impedance, } ^\circ\text{C/W}$$

For the pc board with thermal vias, there are three thermal paths: through the plated copper via annulus, through any solder that might fill the via, and through the epoxy fiberglass of the pc board. The thermal conductivity of the epoxy fiberglass material is almost two orders of magnitude smaller than the thermal conductivity of the solder and the copper, so its contribution is ignored. Equation 4 then becomes:

$$5) \quad \theta_{pcb} = \Delta x / (k_{eq} * A_{eq})$$

$$\text{Where } k_{eq} * A_{eq} = (k_{cu} * A_{cu} + k_{sldr} * A_{sldr})$$

$$k_{cu} = 0.390 \text{ W/m}^\circ\text{C}$$

$$A_{cu} = \text{Area of 0.25 mm diameter via plated with 38 microns of Cu.}$$

$$k_{cu} * A_{cu} = 0.0136 \text{ W*mm}^\circ\text{C}$$

$$k_{sldr} = .050 \text{ W/m}^\circ\text{C}$$

$$A_{sldr} = \text{area of 0.25 mm diameter via filled with solder.}$$

$$k_{sldr} * A_{sldr} = 0.0025 \text{ W*mm}^\circ\text{C}$$

For a 1.6 mm thick pc board, the thermal impedance is 99  $^\circ\text{C/W}$  for a single via that is filled with solder. If the contribution of the solder is excluded, the thermal impedance of the via alone is only 117  $^\circ\text{C/W}$ . With this information, the user can determine the number of vias required for the application. For the WJ AH201 33 vias are recommended. The thermal impedance is then 3  $^\circ\text{C/W}$  with solder filled vias and 3.5

°C/W for vias without solder. Solder filling the vias provides only a small benefit. Most of the heat transfer is provided by the copper.

Unfortunately, assumptions that power is uniformly spread over the die paddle and that the die paddle is isothermal are simplifying approximations. Generally, the die is smaller than the paddle so the die paddle is not isothermal. In this case, a finite element model of the geometry must be prepared to accurately model the problem. The WJ AH201 provides a good example. The die dissipates power over a region that is 1 mm x 1 mm centered on the 4 mm x 4 mm paddle. A finite element model of the AH201 was prepared using COSMOS/<sup>TM</sup> FEA software to analyze the thermal impedance of the package assembly through the WJ-recommended pc board.

The model, shown in Figure 8, is a quarter model of the QFN package, a 75 micron solder joint, and a 4-layer 1.6 mm thick FR-4 pc board with 1 oz. copper and 33 0.25 mm diameter vias. Four scenarios were analyzed. The first and second scenarios consist of the power spread over a 1 mm x 1 mm section on the top of the copper paddle in the QFN package. In the first scenario the vias were filled with solder, and in the second scenario the vias were not filled. The third and fourth scenarios assumed that the power was uniformly spread over the entire 4 mm x 4 mm top surface of the QFN package. The vias were filled with solder in the third scenario, and the vias were unfilled in the fourth scenario. Scenarios three and four were included to evaluate the accuracy of the closed-form solution presented in Equation 5. The resulting thermal profiles for scenarios 1 and 3 are shown in Figure 9 and Figure 10 respectively.

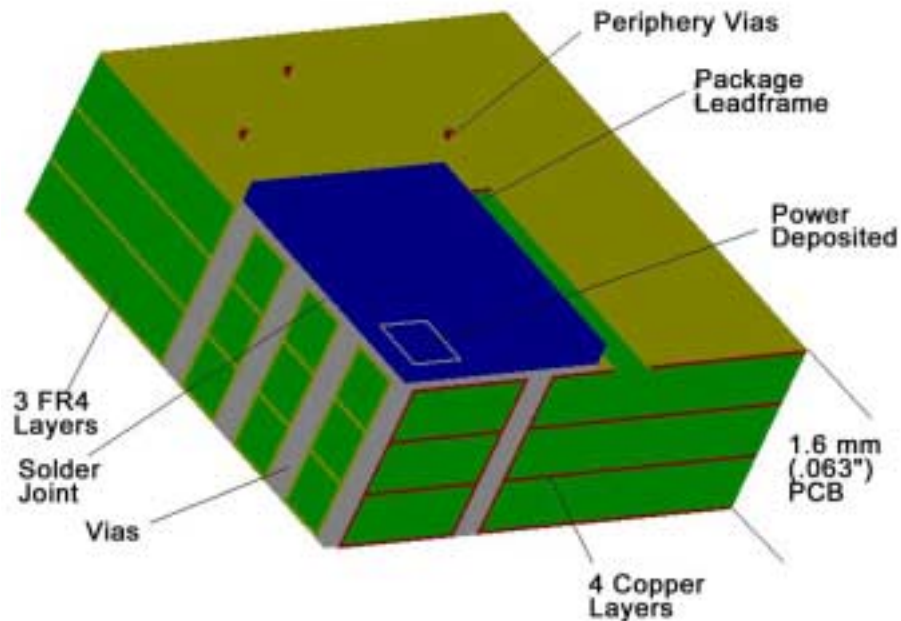
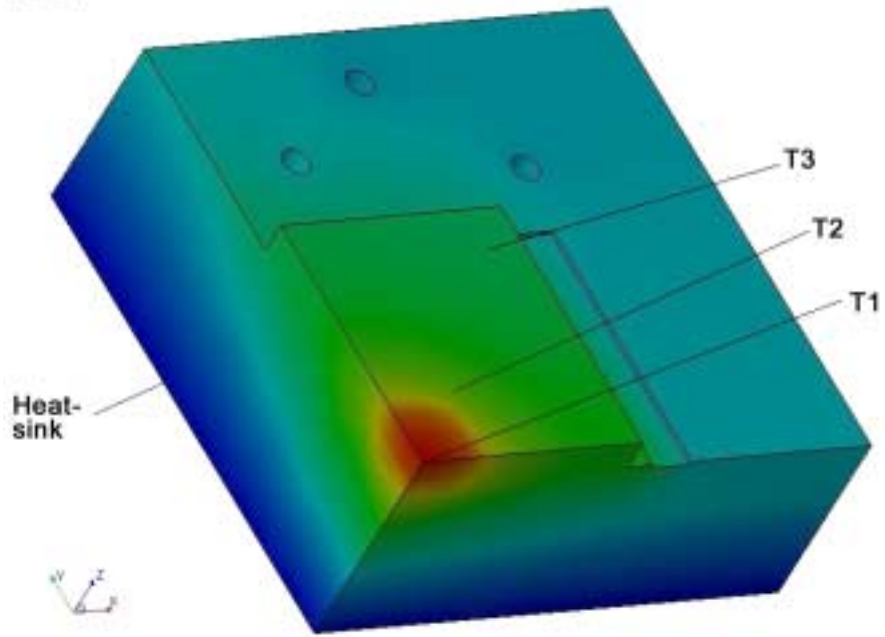
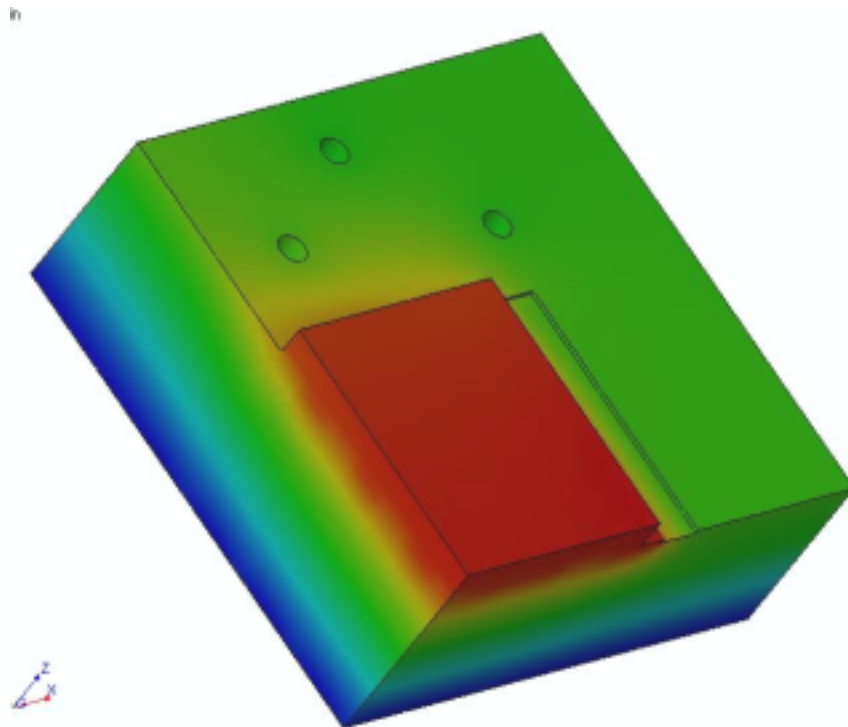


Figure 8: Finite Element Analysis (FEA) Model of the WJ AH201 Amplifier Mounted on a pc board

Fig.10\_Corvedon : Thermal Time step: 1  
Units: Kelvin



**Figure 9: Thermal Gradients Computed for the AH201 Model**



**Figure 10: Thermal Gradients Computed for the Isothermal Model**



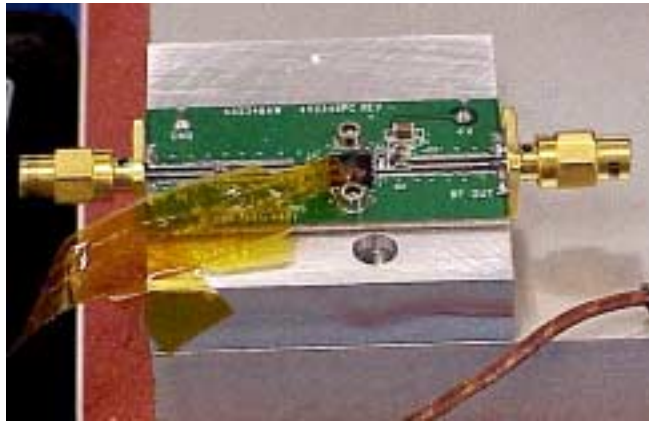
The results are summarized in Table 1. Thermal impedance was calculated at three points on the model. Point 1 is the center of the pc board, underneath the package and solder joint. This should be the hottest point on the pc board since it is directly underneath the die. Point 2 is on the pc board between the outer corner of the paddle and the center of the paddle and point 3 is on the pc board near the edge of the paddle. For the isothermal analyses (scenarios 3 and 4), the thermal impedance is constant across the back of the package. It is important to note that because of the high power concentration in the center of the package for Scenarios 1 and 2, the thermal impedance is much higher locally in this area. However, because the thermal impedance of the package is reported as the temperature difference between the device junction and the outer edge of the package, the user only needs to be concerned with the temperature difference between the outer edge of the paddle and the backside of the pc board. This is point 3 in the table. It is also interesting to note the good agreement between the results for the closed form calculations and the FEA model for the uniformly distributed power cases. As one would expect, the values predicted by the FEA models are slightly lower than the values calculated by the simplified equation because the FEA model includes the effect of conduction in the x, y and z directions. The one-dimensional conduction model does not.

Condition	Thermal Impedance (deg C/W)		
	Point 1	Point 2	Point 3
Scenario 1: WJ AH201 with solder filled vias	5.0	3.0	2.3
Scenario 2: WJ AH201 with no solder in vias	5.4	3.5	2.5
Scenario 3: Power spread uniformly over die paddle; solder filled vias	2.7	2.7	2.7
Scenario 4: Power spread uniformly over die paddle; no solder in vias	3.1	3.1	3.1
Equation 5: solder in vias	3.0	3.0	3.0
Equation 5: no solder in vias	3.5	3.5	3.5
Measured data	N/A	2.5	N/A

**Table 1: Summary of thermal impedance computations**

To validate the analytical models, testing was performed on a WJ AH201 device mounted on the WJ-recommended pc board. The vias were filled with solder. A small hole was drilled into the top of the AH201 as close to the die as practical so that the copper ground paddle was exposed. A K type thermocouple having 3 mil diameter wires was then epoxied to the paddle. This position roughly corresponds to Point 2 in Table 1. The pc

board was mounted to a temperature-controlled heat plate that was maintained at a constant temperature. A thermocouple was attached to the heat plate as close to the board as possible to record the temperature at the top of the heat plate. The temperature difference between the thermocouple on the top of the paddle and the thermocouple on the temperature plate was used to determine the thermal impedance of the pc board. The measured data shows a thermal impedance of  $2.5\text{ }^{\circ}\text{C}/\text{W}$ . This is lower than predicted by scenario 1 by about  $.5\text{ }^{\circ}\text{C}/\text{W}$ . The difference is probably due to the fact that the actual test board is much larger than the thermal model. There is thermal spreading into the ground plane along the top surface of the test board that reduces the top-side temperature.



**Figure 11: WJ AH201 used to measure thermal impedance of the pc board**

### ***Summary:***

Through proper board and heatsink design it is possible to replace cumbersome and expensive flange mount packages with surface mount packages. This paper shows the pc board designer how to easily determine the thermal impedance of the pc board as a function of the number of thermal vias utilized through the use of a simplified closed-form equation (Equation 5).